Version with markings to show changes made

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Priority Application Serial No. 08/842,230
Priority Filing Date ..... April 22, 1997
Inventor ..... Luan Tran et al.
Assignee ..... Micron Technology, Inc.
Priority Group Art Unit 2814
Priority Examiner .....H. Weiss
Attorney's Docket No. MI22-1784
Title: Memory Integrated Circuitry

37 CFR §1.121(b)(1)(iii) AND 37 CFR §1.121(c)(1)(ii) FILING REQUIREMENTS TO ACCOMPANY PRELIMINARY AMENDMENT

Deletions are bracketed, additions are underlined.

In the Specification

At page 1, before the **TECHNICAL FIELD** insert:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 08/842,230, filed on April 22, 1997, entitled "Memory Integrated Circuitry" and naming Luan Tran and Alan R. Reinberg as inventors, the disclosure of which is hereby incorporated herein by reference.

The paragraph beginning at p. 9, line 22 and extending through p. 9, line 23 has been amended as shown below:

U.S. patent application serial number 08/530,661 listing Brent Keeth and Pierre Fazan as inventors [is] discloses methods which can be utilized for forming the structures disclosed herein (such as, for example, dry oxidation for formation of LOCOS), and is hereby incorporated by reference.

At p. 11, line 2, after CLAIMS, We claim: has been inserted.

In the Claims

3. (Amended) The memory integrated circuitry of claim 1 wherein individual ones of the lines of memory cells are substantially straight throughout the array.

7. (Amended) Memory integrated circuitry comprising:

an array of memory cells formed over a semiconductive substrate and occupying area thereover, at least some memory cells of the array being formed in lines of active area formed within the semiconductive substrate which are continuous between adjacent memory cells, said adjacent memory cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent memory cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween.

8. (Amended) The memory integrated circuitry of claim 7 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

13. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is no greater than 0.25 micron and is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

at least some of the minimum pitch adjacent lines of memory cells within the array being isolated from one another by LOCOS field oxide formed therebetween; and

the bit lines comprise D and D^* lines formed in a folded bit line architecture within the array.

14. (Amended) The memory integrated circuitry of claim 13 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

18. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a bulk silicon semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, the word lines and bit lines having respective conductive widths which are less than or equal to 0.25 micron, the DRAM cells within the array being formed in lines of active area formed within the silicon substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by respective conductive lines formed over said continuous active area between said adjacent DRAM cells;

at least some adjacent lines of continuous active area within the array being isolated from one another by LOCOS field oxide formed therebetween, said LOCOS field oxide having a thickness of no greater than 2500 Angstroms;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than 0.5 micron^2; and

the bit lines comprise D and D* lines formed in a folded bit line architecture within the array.

19. (Amended) The memory integrated circuitry of claim 18 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

22. (Amended) Dynamic random access memory circuitry comprising:

an array of word lines and bit lines formed over a semiconductive substrate defining an array of DRAM cells occupying area over the semiconductive substrate, at least some DRAM cells of the array being formed in lines of active area formed within the semiconductive substrate beneath the word lines and which are continuous between adjacent DRAM cells, said adjacent DRAM cells being isolated from one another relative to the continuous active area formed therebetween by a conductive line formed over said continuous active area between said adjacent DRAM cells;

the respective area consumed by individual ones of said adjacent memory cells being equal to less than $8F^2$, where "F" is defined as equal to one-half of minimum pitch, with minimum pitch being defined as equal to the smallest distance of a line width plus width of a space immediately adjacent said line on one side of said line between said line and a next adjacent line in a repeated pattern within the array; and

the bit lines comprise D and D^* lines formed in a folded bit line architecture within the array.

23. (Amended) The memory integrated circuitry of claim 22 wherein individual ones of the lines of continuous active area are substantially straight throughout the array.

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